AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method comprising:

providing a wafer comprised of a bulk substrate, an insulating layer positioned above said bulk substrate, and a semiconducting layer positioned above said insulating layer;

forming an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate;

forming a patterned layer of photoresist above said exposed surface area of said bulk substrate;

[[forming]] performing at least one etching process to form an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate using said patterned layer of photoresist as a mask for said at least one etching process; and

forming a layer of material above said alignment mark and in said opening.

2. (Previously Presented) The method of claim 1, wherein providing a wafer comprised of a bulk substrate, an insulating layer positioned above said bulk substrate, and a semiconducting layer positioned above said insulating layer comprises providing a wafer comprised of a bulk substrate comprised of at least one of silicon, silicon nitride, gallium arsenide, and silicon germanium.

3. (Original) The method of claim 1, wherein providing a wafer comprises providing a wafer having a diameter of at least one of approximately 4 inches, 8 inches and 12 inches.

4. (Original) The method of claim 1, wherein forming an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate comprises performing at least one etching process to form an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate.

5. (Canceled)

6. (Original) The method of claim 1, wherein forming a layer of material above said alignment mark and in said opening comprises depositing a layer of material above said alignment mark and in said opening.

7. (Original) The method of claim 1, wherein forming a layer of material above said alignment mark and in said opening comprises forming a layer of material comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than approximately 8.0 above said alignment mark and in said opening.

8. (Original) The method of claim 1, further comprising performing a planarization operation after forming said material above said alignment mark and in said opening.

9. (Original) The method of claim 1, further comprising:

positioning said wafer in a photolithography stepper tool; and

reflecting a light off of said alignment mark formed in said bulk substrate to properly position said wafer for processing in said photolithography stepper tool.

10. (Original) The method of claim 1, wherein forming an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate comprises forming a plurality of openings in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate within each of said openings.

11. (Original) The method of claim 10, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate in each of said openings.

12. (Original) The method of claim 1, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises forming an alignment mark comprised of a plurality of grating structures in said bulk substrate within said exposed surface area of said bulk substrate.

13. (Withdrawn) A method comprising:

providing a wafer comprised of a bulk silicon substrate, an insulating layer positioned above said bulk substrate, and a semiconducting layer comprised of silicon positioned above said insulating layer;

performing at least one etching process to form an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate;

forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate; and

forming a layer of material above said alignment mark and in said opening.

14. (Withdrawn) The method of claim 13, wherein providing a wafer comprises providing a wafer having a diameter of at least one of approximately 4 inches, 8 inches and 12 inches.

15. (Withdrawn) The method of claim 13, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises:

forming a patterned layer of photoresist above said exposed surface area of said bulk substrate; and

performing at least one etching process to form said alignment mark in said exposed surface area of said bulk substrate using said patterned layer of photoresist as a mask.

16. (Withdrawn) The method of claim 13, wherein forming a layer of material above said alignment mark and in said opening comprises depositing a layer of material above said alignment mark and in said opening.

17. (Withdrawn) The method of claim 13, wherein forming a layer of material above said alignment mark and in said opening comprises forming a layer of material comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than approximately 8.0 above said alignment mark and in said opening.

18. (Withdrawn) The method of claim 13, further comprising performing a planarization operation after forming said material above said alignment mark and in said opening.

19. (Withdrawn) The method of claim 13, further comprising:

positioning said wafer in a photolithography stepper tool; and

reflecting a light off of said alignment mark formed in said bulk substrate to properly position said wafer for processing in said photolithography stepper tool.

20. (Withdrawn) The method of claim 13, wherein performing at least one etching process to form an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate comprises performing at least one etching process to form a plurality of openings in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate within each of said openings.

21. (Withdrawn) The method of claim 20, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises forming an

alignment mark in said bulk substrate within said exposed surface area of said bulk substrate in each of said openings.

22. (Withdrawn) The method of claim 13, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises forming an alignment mark comprised of a plurality of grating structures in said bulk substrate within said exposed surface area of said bulk substrate.

23. (Withdrawn) A method comprising:

providing a wafer comprised of a bulk silicon substrate, an insulating layer comprised of a material having a dielectric constant less than approximately 8.0 positioned above said bulk substrate, and a semiconducting layer comprised of silicon positioned above said insulating layer;

performing at least one etching process to form an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate;

forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate; and

depositing a layer of material above said alignment mark and in said opening.

24. (Withdrawn) The method of claim 23, wherein providing a wafer comprises providing a wafer having a diameter of at least one of approximately 4 inches, 8 inches and 12 inches.

25. (Withdrawn) The method of claim 23, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises:

forming a patterned layer of photoresist above said exposed surface area of said bulk substrate; and

performing at least one etching process to form said alignment mark in said exposed surface area of said bulk substrate using said patterned layer of photoresist as a mask.

26. (Withdrawn) The method of claim 23, wherein depositing a layer of material above said alignment mark and in said opening comprises depositing a layer of material comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than approximately 8.0 above said alignment mark and in said opening.

27. (Withdrawn) The method of claim 23, further comprising performing a planarization operation after depositing said material above said alignment mark and in said opening.

28. (Withdrawn) The method of claim 23, further comprising:

positioning said wafer in a photolithography stepper tool; and

reflecting a light off of said alignment mark formed in said bulk substrate to properly position said wafer for processing in said photolithography stepper tool.

29. (Withdrawn) The method of claim 23, wherein performing at least one etching process to form an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate comprises performing at least one etching process to form a plurality of openings in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate within each of said openings.

30. (Withdrawn) The method of claim 29, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate in each of said openings.

31. (Withdrawn) The method of claim 23, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises forming an alignment mark comprised of a plurality of grating structures in said bulk substrate within said exposed surface area of said bulk substrate.

32. (Withdrawn) A wafer, comprising:

a bulk substrate;

an insulating layer positioned above said bulk substrate;

a semiconducting layer positioned above said insulating layer;

an opening formed in said semiconducting layer and said insulating layer;

an alignment mark formed in said bulk substrate within an area defined by said opening; and

a layer of material positioned above said alignment mark and within said opening.

33. (Withdrawn) The wafer of claim 32, wherein said bulk substrate comprised of at least one of silicon, silicon nitride, gallium arsenide and silicon germanium.

34. (Withdrawn) The wafer of claim 32, wherein said insulating material is comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than 8.0.

35. (Withdrawn) The wafer of claim 32, wherein said semiconducting layer is comprised of at lest one of silicon, gallium arsenide and silicon germanium.

36. (Withdrawn) The wafer of claim 32, wherein said bulk substrate is comprised of silicon and wherein said semiconducting layer is comprised of silicon.

37. (Withdrawn) The wafer of claim 32, wherein said opening is formed by performing at least one etching process.

38. (Withdrawn) The wafer of claim 32, wherein said alignment mark is comprised of a plurality of grating structures.

39. (Withdrawn) The wafer of claim 32, wherein said layer of material positioned above said alignment mark and within said opening is comprised of at least one of silicon

dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than 8.0.

40. (Withdrawn) A wafer, comprising:

a bulk substrate comprised of silicon;

an insulating layer comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than 8.0 positioned above said bulk substrate;

a semiconducting layer comprised of silicon positioned above said insulating layer;

an opening formed in said semiconducting layer and said insulating layer;

an alignment mark formed in said bulk substrate within an area defined by said opening; and

a layer of material positioned above said alignment mark and within said opening.

41. (Withdrawn) The wafer of claim 40, wherein said opening is formed by performing at least one etching process.

42. (Withdrawn) The wafer of claim 40, wherein said alignment mark is comprised of a plurality of grating structures.

43. (Withdrawn) The wafer of claim 40, wherein said layer of material positioned above said alignment mark and within said opening is comprised of at least one of silicon

dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than 8.0.

44. (New) The method of claim 1, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of silicon positioned above said insulating layer.

45. (New) The method of claim 1, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of gallium arsenide positioned above said insulating layer.

46. (New) The method of claim 1, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of silicon germanium positioned above said insulating layer.

47. (New) A method comprising:

providing a wafer comprised of a bulk substrate, an insulating layer positioned above said bulk substrate, and a semiconducting layer positioned above said insulating layer;

forming an opening in said semiconducting layer and said insulating layer to thereby expose an unpatterned surface area of said bulk substrate;

forming a patterned layer of photoresist above said exposed unpatterned surface area of said bulk substrate;

performing at least one etching process to form an alignment mark in said bulk substrate within said exposed unpatterned surface area of said bulk substrate using said patterned layer of photoresist as a mask for said at least one etching process; and

forming a layer of material above said alignment mark and in said opening.

48. (New) The method of claim 47, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of silicon positioned above said insulating layer.

49. (New) The method of claim 47, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of gallium arsenide positioned above said insulating layer.

50. (New) The method of claim 47, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of silicon germanium positioned above said insulating layer.

51. (New) The method of claim 47, wherein forming the alignment mark in said bulk substrate within said exposed unpatterned surface area of said bulk substrate comprises:

forming a patterned layer of photoresist above said exposed unpatterned surface area of said bulk substrate; and

performing at least one etching process to form said alignment mark in said exposed unpatterned surface area of said bulk substrate using said patterned layer of photoresist as a mask.

52. (New) The method of claim 47, wherein forming the layer of material above said alignment mark and in said opening comprises depositing a layer of material above said alignment mark and in said opening.

53. (New) The method of claim 47, wherein forming the layer of material above said alignment mark and in said opening comprises forming a layer of material comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than approximately 8.0 above said alignment mark and in said opening.

54. (New) The method of claim 47, further comprising performing a planarization operation after forming said material above said alignment mark and in said opening.

55. (New) The method of claim 47, further comprising:

positioning said wafer in a photolithography stepper tool; and

reflecting a light off of said alignment mark formed in said bulk substrate to properly position said wafer for processing in said photolithography stepper tool.

56. (New) The method of claim 47, wherein forming the opening in said semiconducting layer and said insulating layer to thereby expose the unpatterned surface area of said bulk substrate comprises forming a plurality of openings in said semiconducting layer and said insulating layer to thereby expose an unpatterned surface area of said bulk substrate within each of said openings.

57. (New) The method of claim 56, wherein forming the alignment mark in said bulk substrate within said exposed unpatterned surface area of said bulk substrate comprises forming an alignment mark in said bulk substrate within said exposed unpatterned surface area of said bulk substrate in each of said openings.

58. (New) The method of claim 47, wherein forming the alignment mark in said bulk substrate within said exposed unpatterned surface area of said bulk substrate comprises forming an alignment mark comprised of a plurality of grating structures in said bulk substrate within said exposed unpatterned surface area of said bulk substrate.